REMARKS

The Office Action dated May 17, 2006 has been received and carefully noted. The above claims, and the following remarks, are submitted as a full and complete response thereto. Claims 1-18 are pending and submitted for consideration.

Claims 1-3, 11, and 12 stand rejected under 35 U.S.C. §103(a) as being obvious over *Chen* (US Patent No. 6,501,758) in view of *Yamamoto* (US Patent No. 6,658,017). The Office Action took the position that *Chen* teaches each and every element recited in claims 1-3, 11, and 12 except for the packet pool memory. However, the Office Action cites to *Yamamoto* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 1-3, 11, and 12.

Claim 1 recites a memory management unit for a network switch fabric for forwarding data. The memory management unit includes an ingress port interface receiving portions of a data packet, an egress port interface, connected to ingress ports of the fabric through an ingress bus ring, a cell packer, where the cell packer groups packet data into cells, a packet pool memory, where the packet pool memory stores cells received from the cell packer and a cell unpacker, where the cell unpacker separates stored cells before releasing the cells to an egress port.

Chen teaches a method of transporting asynchronous transfer mode cells and time-division multiplexed information over a common fiber ring. The method includes receiving a plurality of incoming signals comprising asynchronous transfer mode cells, legacy data, or time-division multiplexed information. The method further includes formatting the plurality of incoming signals into a first plurality of incoming transport signals comprising asynchronous transfer mode cells and a second plurality of incoming transport signals comprising time-division multiplexed information, and then constructing a first outgoing synchronous transfer mode signal comprising at least one asynchronous transfer mode cell. The method also includes constructing a second outgoing synchronous transfer mode signal comprising time-division multiplexed information, and transmitting the first and second outgoing synchronous transfer mode signals over a common fiber ring.

Yamamoto teaches a control process that enables improved transmission efficiency. When a signal stored in a buffer is outputted by specifying a certain transmission channel, the network is adapted so that the control waits until the buffer has been brought into a state in which the signal can be outputted therefrom to the specified transmission channel.

However, neither *Chen* nor *Yamamoto* teach, show, or suggest a memory management unit having an ingress port interface and an egress port interface that is connected to the ingress ports of the fabric through an ingress bus ring that is part of the switch fabric, as recited in Applicant's independent claim 1, the independent claim from

which claims 2-3, 11, and 12 depend. Figures 2 and 3 of the present application illustrate that the ingress bus ring is internal to the switch fabric and ties the ports and the memory management units together. Additionally, all of the cell packing and unpacking, as well as the packet pool memory, reside in the switch fabric and allow for temporary storage of packet data while the packet is being processed. In contrast, in *Chen*, the system 10 has a fiber ring 12 that connects nodes 14. Column 2, lines 33-36, discloses that the "[f]iber ring 12 may be configured as a synchronous optical network (SONET), as a synchronous digital hierarchy (SDH) network, or other optical network configuration." Such a ring connects network switches together is not an internal bus ring. Additionally, claim 1 recites "an ingress bus ring," which is distinct from the ring discussed in *Chen*, and the *Chen* ring is not taught, disclosed, or suggested as being specific to the ingress of any network node. Therefore, Applicants submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every element recited in Applicant's independent claim 1. As such, reconsideration and withdrawal of the rejection of claim 1, along with each claim depending therefrom, is respectfully requested.

Further, although the Office Action has taken the position that claim 1 does not specifically recite that the ingress bus ring is within the switch fabric, and therefore, the ingress bus ring need not be expressly shown inside the switch fabric in the cited prior art, Applicants respectfully disagree. Applicants submit that the preamble of claim 1 recites "A memory management unit for a network switch fabric ... comprising," and

then the remainder of the claim recites the elements of the switch fabric, including the ingress bus ring. Since the preamble of the claim recites that the claim is specifically directed to the switch fabric, and the claim then recites that one of the elements of the switch fabric is the ingress bus ring, Applicants submit that the Office Action's conclusion that the ingress bus ring is not part of the switch fabric in Applicants' claim is clearly misplaced and unsupported by both the express language of the preamble and claim. Applicants further submit that the Office Action's position that the ingress bus ring is not within the switch fabric is also not aligned with the case law regarding claim interpretation, and as such, constitutes clear error in the interpretation of Applicant's claim and the application of §103 to the present claims. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1, along with each claim depending therefrom.

Claim 5 stands rejected under 35 U.S.C. §103(a) as being obvious over *Chen* and *Yamamoto*, further in view of *Bass* (US Patent No. 6,862,292). The Office Action took the position that *Chen* and *Yamamoto* teach each and every element recited in claim 5, except for the egress scheduler communicating with the cell unpacker. However, the Office Action cites to *Bass* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of

references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claim 5.

Chen and *Yamamoto* are discussed above. *Bass* teaches a method and system for scheduling the egress of processed information units from a network processing unit according to stored priorities associated with the various sources of the information units. The priorities include a low latency service, a minimum bandwidth, a weighted fair queuing, and a system for preventing a user from continuing to exceed his service levels over an extended period. A plurality of calendars with different service rates to allow a user to select the service rate desired are included. If a user has chosen a high bandwidth for service, the user will be included in a calendar which is serviced more often than if the user has chosen a lower bandwidth.

However, *Bass* does not teach, show, or suggest a memory management unit having an ingress port interface and an egress port interface that is connected to the ingress ports of the fabric through an ingress bus ring that is part of the switch fabric, as recited in Applicants' independent claim 1, the claim from which claim 5 depends. As such, Applicants submit that *Bass* fails to further the teaching of *Chen* and *Yamamoto* to the level necessary to support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claim 5 is respectfully requested.

Claims 7 and 8 stand rejected under 35 U.S.C. §103(a) as being obvious over *Chen*, *Yamamoto*, and *Bass*, further in view of *Stilladis* (US Patent No. 6,134,217). The Office Action took the position that *Chen* and *Yamamoto* teach each and every element

recited in claim 5, except for the priority rules comprising a deficit round robin algorithm.. However, the Office Action cites to *Stilladis* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 7 and 8.

Chen, *Yamamoto*, and *Bass* are discussed above. *Stilladis* a teaches traffic scheduling system for providing quality-of-service (QoS) guarantees in a packet-switched communication network where multiple traffic sessions share an outgoing communication link of a network switch such that a minimum rate is reserved for each session sharing the link. In the system, a packet arriving for transmission on an outgoing link of the switch is assigned a timestamp and placed in a priority queue in the order of increasing timestamps so that the packet with the smallest timestamp is placed at the head of the queue.

However, *Stilladis* does not teach, show, or suggest a memory management unit having an ingress port interface and an egress port interface that is connected to the ingress ports of the fabric through an ingress bus ring that is part of the switch fabric, as recited in Applicants' independent claim 1, the claim from which claims 7 and 8 depend. As such, Applicants submit that *Stilladis* fails to further the teaching of *Chen*, *Yamamoto*, and *Bass* to the level necessary to support an obviousness rejection. Therefore,

reconsideration and withdrawal of the rejection of claims 7 and 8 is respectfully requested.

Claim 10 stands rejected under 35 U.S.C. §103(a) as being obvious over *Chen* and *Yamamoto*, and further in view of *Roy* (U.S. Patent No. 6,243,359). The Office Action took the position that *Chen* and *Yamamoto* teach each and every element recited in claim 10, except for queues configured to determine if a class of service class in the transaction queues has reached a limit and purge the data packet when the transaction queue has reached the limit. However, the Office Action cites to *Roy* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claim 10.

Chen and *Yamamoto* are discussed above. *Roy* teaches a communication device having a separate line side inlet queue for each GFR VC, a single network side outlet queue for all GFR VCs, a single network side inlet queue for all GFR VCs, a single line side outlet bulk processing queue with a post queue packet processor followed by separate line side outlet queues for each line, a network side outlet queue monitor, and a line side inlet queue controller. The network side outlet queue monitor is coupled to the line side inlet queue controller so that the network side outlet queue monitor can send messages to the line side inlet queue controller.

However, *Roy* does not does not teach, show, or suggest a memory management unit having an ingress port interface and an egress port interface that is connected to the ingress ports of the fabric through an ingress bus ring that is part of the switch fabric, as recited in Applicants' independent claim 1, the claim from which claim 10 depends. As such, Applicants submit that *Roy* fails to further the teaching of *Chen* and *Yamamoto* to the level necessary to support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claim 10 is respectfully requested.

Claim 13 stands rejected under 35 U.S.C. §103(a) as being obvious over *Chen* and *Yamamoto*, further in view of *Haraszti* (U.S. Patent No. 5,612,964). The Office Action took the position that *Chen* teaches each and every element recited in claim 13, except for the memory error detector and a means for recovering from the error. However, the Office Action cites to *Haraszti* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claim 13.

Chen and *Yamamoto* are discussed above. *Haraszti* teaches a high performance fault tolerant orthogonal shuffle memory comprising a plurality of memory cells arranged to form a two-dimensional array of rows and columns. Each memory cell includes a data store element for storing data and a multi-state data transmission element to provide

access to the data stored in the data store element. Each memory cell has the dual function of storing and transmitting or shifting data. The memory cell array is coupled to first and second registers and a shuffle signal generator.

However, *Haraszti* does not does not teach, show, or suggest a memory management unit having an ingress port interface and an egress port interface that is connected to the ingress ports of the fabric through an ingress bus ring that is part of the switch fabric, as recited in Applicants' independent claim 1, the claim from which claim 13 depends. As such, Applicants submit that *Haraszti* fails to further the teaching of *Chen* and *Yamamoto* to the level necessary to support an obviousness rejection. Therefore, reconsideration and withdrawal of the rejection of claim 13 is respectfully requested.

Claim 14 and 17 stand rejected under 35 U.S.C. §103(a) as being obvious over *Chen* and *Yamamoto*, further in view of *Dai* (U.S. Patent No. 6,658,016). The Office Action took the position that *Chen* and *Yamamoto* teach each and every element recited in claims 14 and 17, except for the packet switching fabric containing the memory management unit and the configuration of the ring. However, the Office Action cites to *Dai* as teaching these features, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in

combination, fails to teach, show, or suggest each and every limitation recited in claims 14 and 17.

Chen and *Yamamoto* are discussed above. *Dai* teaches a packet switching fabric having a data ring, a control ring, and a plurality of data communication network links each having at least one network node coupled thereto. The fabric further includes a plurality of output queuing controlled switching devices coupled together by the data ring and the control ring, so that the network links can be selectively coupled. Each of the output queuing controlled switching devices includes control ring processor operative to develop, transmit, and receive control messages to and from adjacent ones of the devices via the control ring. The control messages provide for controlling packet transfer operations including transmitting associated selected ones of the received data packets from the associated source device to the associated destination device via an associated source-destination channel path including associated ones of the data ring segments and an associated one of the memory unit links.

However, *Dai* does not does not teach, show, or suggest a memory management unit having an ingress port interface and an egress port interface that is connected to the ingress ports of the fabric through an ingress bus ring that is part of the switch fabric, as recited in Applicants' independent claim 1, the claim from which claims 14 and 17 depend. As such, Applicants submit that *Dai* fails to further the teaching of *Chen* and *Yamamoto* to the level necessary to support an obviousness rejection. Therefore,

reconsideration and withdrawal of the rejection of claims 14 and 17 is respectfully requested.

In conclusion, Applicants submit that the cited combination of references fails to teach, show, or suggest each and every limitation recited in Applicants' independent claim 1, the independent claim from which each of claims 2-18 depend. Therefore, Applicants submit that each of claims 1-18 recites subject matter that is not taught, disclosed, or otherwise suggested by the cited combination of references. As such, reconsideration and withdrawal of the rejection of claims 1-18 is respectfully requested. Claims 1-18 are pending and submitted for consideration.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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